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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,093	03/23/2004	Amar Guettaf	1875.4450000	1879
26111 7590 05/16/2007 STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER RADOSEVICH, STEVEN D	
			ART UNIT 2117	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/806,093	Applicant(s) GUETTAF, AMAR	
	Examiner Steven D. Radosevich	Art Unit 2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 March 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) 8 and 21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7, 9-20 and 22-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 August 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/19/07 has been entered. Claims 1-28 are present within this instant examination of the application.

Response to Arguments

Applicant's arguments filed 3/19/07 have been fully considered but they are not persuasive.

Applicant directed the examiner to paragraph 0043 to overcome the 35 U.S.C 112 second paragraph rejection with respect to it being unclear to the examiner how, as specified in claims 1(a) and 17(a), "...other scan paths within the plurality of scan paths...considered to be good scan paths..." can contribute to test results that effect, as specified in (original) claims 1(e) and 17(f), "...tracing the source of errors of the bad scan path...". And how these test results would further effect, as specified in (original) claims 1(f) and 17(g), "shifting the segment point of the bad scan path...". Examiner notes that paragraph 0043 does not explain how the good scan paths contribute to test result that effect tracing the source of errors of the bad scan path, the paragraph in-fact furthers the misunderstanding since the paragraph indicates the bad path is not in error or bad and that the considered to be good scan paths are bad or in error once a

segment point is established. The paragraph 0043 is included below which corresponds to figure 2 within the application:

If on the other hand, scan path 220 output does not exceed the bad path error threshold amount, and the number of errors on good scan paths 220 and 240 exceed a good path error threshold amount, then the segment point is shifted to the left. In one embodiment, the shift is done by once again dividing the number of flip-flops between the start of the scan path and the current segment point in half to determine the next segment point. For example, the segment point A is shifted to a new segment point C located between flip-flop 223 and 224 within scan path 220, such that three flip-flops are located between point A and C, and three are located between point C and the input of scan path 200.

As the paragraph indicates the bad scan path is identified to be path 220 while the good scan paths are identified to be 200 and 240 which are not "good scan paths" since they contain errors that exceed a good scan path error threshold while the segmented "bad path" 220 does not exceed the bad path threshold, indicating it is good, while the "good scan paths" 200 and 240 effect the segmentation of the "bad path" 220 so that the errors within the "bad path" 220 can be isolated/located/identified/debugged. It remains unclear as to how the good scan paths can contribute to test results that effect the tracing of the source of errors of the bad scan path. Examiner notes the "bad path" 220 will be segmented until eliminated from examination if the "good scan paths" are used to further the segmentation point within the "bad path" 220.

Examiner as per claims 1 and 17 retains the 35 U.S.C. 112 second paragraph rejections along with the 35 U.S.C. 103 since these claims remain unclear and indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-7, 9-20, and 22-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1 and 17 see the examiner's response to applicant's remarks described above regarding the maintaining of the 35 U.S.C 112 second paragraph rejection of these independent claims for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2-7, 9-16, 18-20, and 22-28 are dependent upon the independent claims 1 and 17 respectfully and therefore also inherit the 35 U.S.C 112 second paragraph issues and may not be further considered upon their merits.

Appropriate correction and or explanation is required to overcome the 35 U.S.C. 112 second paragraph rejection(s).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-7, 10, 20, and 22-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin-de-Nicolas et al (U.S. Publication 2003/0208710) in view of Applicants Admitted Prior Art (AAPA) as described above and as follows in some detail.

1. As per claim 1, Martin-de-Nicolas teaches scan testing of an integrated circuit with a plurality of scan paths, a method of debugging scan testing failures of the integrated circuit, comprising the steps of:

- a. Identifying a bad scan path that is generating one or more errors within the plurality of scan paths (0019 lines 7-9 in addition to 0022 lines 15-19);
- b. Defining a segment point that segments the bad scan path into two segments (0028-0031);
- c. Conducting scan tests on the plurality of scan paths (0019 line 9)
- d. Assessing scan test results on the bad (0018 lines 8-10 and 0022 lines 16-19);

- e. Tracing the source of errors when the number of errors of an output of the bad scan path following the segment point are less than a bad path error threshold (0018 lines 10-12 and 0029); and
- f. Shifting the segment point based on an analysis of the errors generated by the bad scan path and the good scan path and returning to step (b) when the number of errors of an output of the bad scan path are greater than a bad path error threshold (0028-0029 and 0031).

Martin-de-Nicolas does not specifically teach wherein in step (a) all other scan paths within the plurality of scan paths are considered to be good scan paths.

However as noted within the AAPA in paragraph 0005 "when there is a failure within a particular scan path, errors will be generated on the output of that scan path [bad scan path], but also can be propagated to other scan paths [good scan paths] through logical and physical interconnections." Therefore those of ordinary skill in the art at the time the invention was made would recognize that scan chains that produce an error at their output may have produced the errors not because they are bad scan paths but because of their logical and physical interconnections with a bad scan path which produces the error(s).

Therefore those of ordinary skill in the art at the time the invention was made would have been motivated within the method of Martin-de-Nicolas to select a single scan path outputting an error(s) from a number of scan paths outputting an error(s) to be a "bad scan path," while all others are presumed to be "good scan paths," to examine the "bad scan path" with the described binary search method in Martin-de-

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Nicolas so as to quickly determine if that scan path is the scan path producing the error(s) in other scan paths by quickly identifying the faulty location(s) within that scan path and fix, replace, or bypass the faulty circuitry, thus eliminating the error(s) produced within that scan path ("bad scan path") and/or other scan paths ("good scan paths") that only through "logical and physical interconnections with" that bad scan path may output an error(s) which would save time and money since each scan path outputting an error(s) does not need to be examined.

2. As per claims 2 and 18, Martin-de-Nicolas teaches that all the scan paths are tested a number of times with multiply tests confirming which scan paths are faulty and which are not (0019 line 7-9 in addition to 0022 lines 15-19).
3. As per claims 3 and 19, the art is replete with masking of identified faulty scan paths while further testing any remaining unidentified scan paths as faulty with various tests. This method of masking reduces processing time since the identified faulty scan paths are not retested or examined since they are already found to be faulty (0019 lines 7-9).
4. As per claim 4, Martin-de-Nicolas teaches wherein step (a) of claim 1 includes running a series of scan tests for the plurality of scan paths (0019 lines 7-9 in addition to 0022 lines 15-19).
5. As per claims 5-7, Martin-de-Nicolas teaches the above as per claim 1 wherein a number of testes are executed on a plurality of scan paths (0019 lines 7-9 with in addition to 0022 lines 16-19).

Martin-de-Nicolas does not specifically teach wherein these tests executed include varying the temperature of the integrated circuit, frequency of a clock signal input, or the test voltage.

However, as evidenced by the AAPA within the specification of the instant application it was known at the time the invention was made when factors such as frequency, temperature, or voltage are changed, errors within that circuit can be caused (0006).

6. Therefore, the Examiner interprets that the plurality of tests run by Martin-de-Nicolas incorporates these factors of varying the temperature, frequency, and test voltage, wherein these factors are within the limitations in which the circuit is rated to operate since Martin-de-Nicolas desires as does the applicant to identify and locate errors within a DUT (0008, 0019 lines 7-9 with 0029 lines 5-9).

7. As per claims 10 and 22, Martin-de-Nicolas teaches wherein in step (e) of claim 1 and (f) ("I" in this examination) the tracing of errors includes identifying a first error source that generated an error and determining whether the error originated with the first error source (0029). Examiner interprets that "identifying a first error source," is the determining of the location of the error, that error must have originated within "the first error source," since it was identified as the first error source.

8. As per claims 11 and 23, Martin-de-Nicolas teaches wherein the tracing the source of errors is conducted manually (0005 lines 1-3).

9. As per claims 12 and 24, Martin-de-Nicolas teaches wherein the tracing the source of errors is conducted automatically through an automated testing unit (0008).

10. As per claims 13-16 and 25-28, Martin-de-Nicolas teaches the sifting of the segment point midway or in the direction from its present location to the end/beginning of the scan chain dependent on the testing results (0028-0029 and 0031). Examiner notes that this is the implementation of a binary search for locating errors or faults such as taught throughout the publication by Martin-de-Nicolas.

11. As per claim 17, Martin-de-Nicolas teaches scan testing of an integrated circuit with a plurality of scan paths, a method of debugging scan testing failures of the integrated circuit, comprising the steps of:

- g. Identifying a plurality of bad scan paths that is generating one or more errors within the plurality of scan paths (0019 lines 7-9 in addition to 0022 lines 15-19);
- h. Masking all bad scan paths except a bad scan path under test (0019 lines 7-9);
- i. Defining a segment point that segments the bad scan path into two segments (0028-0031);
- j. Conducting scan tests on the plurality of scan paths (0019 line 9);
- k. Assessing scan test results on the bad (0018 lines 8-10 and 0022 lines 16-19);
- l. Tracing the source of errors when the number of errors of an output of the bad scan path under test are less than a bad path error threshold (0018 lines 10-12 and 0029);

m. Shifting the segment point based on an analysis of the errors generated by the bad scan path and the good scan path and returning to step when the number of errors of an output of the bad scan path under test are greater than a bad path error threshold (0028-0029 and 0031); and

n. Repeating steps (b) ("i" in this examination) through (g) ("n" in this examination) until the source or sources of errors within all bad scan paths among said plurality of bad scan paths have been located 0033 lines 6-8).

Martin-de-Nicolas does not specifically teach wherein in step (a) all other scan paths within the plurality of scan paths are considered to be good scan paths.

However as noted within the AAPA in paragraph 0005 "when there is a failure within a particular scan path, errors will be generated on the output of that scan path [bad scan path], but also can be propagated to other scan paths [good scan paths] through logical and physical interconnections." Therefore those of ordinary skill in the art at the time the invention was made would recognize that scan chains that produce an error at their output may have produced the errors not because they are bad scan paths but because of their logical and physical interconnections with a bad scan path which produces the error(s).

Therefore those of ordinary skill in the art at the time the invention was made would have been motivated within the method of Martin-de-Nicolas to select a single scan path outputting an error(s) from a number of scan paths outputting an error(s) to be the "bad scan path," while all others are presumed to be "good scan paths" or masked, to examine the "bad scan path" with the described binary search method in

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Martin-de-Nicolas so as to quickly determine if that scan path is the scan path producing the error(s) in other scan paths by quickly identifying the faulty location(s) within that scan path and fix, replace, or bypass the faulty circuitry, thus eliminating the error(s) produced within that scan path ("bad scan path") and/or other scan paths ("good scan paths") that only through "logical and physical interconnections with" that bad scan path may output an error(s) which would save time and money since each scan path outputting an error(s) does not need to be examined.

12. As per claim 20, Martin-de-Nicolas teaches wherein step (a) of claim 17 ("g" in this examination) includes running a series of scan tests for the plurality of scan paths (0019 lines 7-9 in addition to 0022 lines 15-19).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Martin-de-Nicolas (2003/0208710) in view of AAPA as applied to claim 1 above, and further in view of Akita (5541940) or Sugimoto et al. (6999386).

13. As per claim 9, Martin-de-Nicolas teaches the above as per claim 1 wherein a binary search is performed to locate the error or failure.

Martin-de-Nicolas does not specifically teach wherein in step (d) there is included a determination of the number of errors generated by the bad scan path following the segment point and each of the good scan paths.

However in the analogous arts of both Akita and Sugimoto it is taught that it is important to determine the number of errors generated from a DUT.

Therefore, one of ordinary skill in the art at the time the invention was made would have been motivated to combine the binary search as taught by Martin-de-

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Nicolas by adding to it determining of the number of errors generated by a DUT as taught by either Akita or Sugimoto so that a determination of whether or not the number of errors exceeds the capacity of the system may be made and so that all detected errors are located if the number of errors falls within the capacity of the system to do so.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- i. Bhavsar et al. (U.S. Patent 6260166) discloses a binary search in an efficient production test and debug architecture.
- ii. Wilson et al. (U.S. Patent 5210486) discloses a binary search within a circuit test method.
- iii. Koo et al. (U.S. Patent 5386423) discloses a binary search used within testing.
- iv. Lindberg et al. (U.S. Patent 5663967) discloses a binary search used within scan-path testing and probing.
- v. Klaiber et al. (U.S. Patent 5905855) discloses a binary search used to rapidly narrow the search for an error.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Cynthia H. Britt can be reached on 571-2723815. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


CYNTHIA BRITT
PRIMARY EXAMINER

Steven D. Radosevich
Examiner
Art Unit 2117

